IN THE CLAIMS

Please Amend the Claims in accordance with the following mark-up copy:

1. (Currently Amended) A comparator circuit, comprising:

a pair of differential inputs for receiving a differential data signal pair;

a single-ended input for receiving a single-ended data signal;

a reference combiner, whereby a reference value for detecting said single-ended data signal is derived in conformity with analog values of both signals of said differential data signal pair; and

a single-ended comparator for comparing an analog value of said single-ended data signal with said reference value, and having an output representative of a digital binary state of said single-ended data signal, whereby said single-ended signal is detected in conformity with a common mode value of said differential data signal pair~~; and~~

~~a differential comparator for comparing said analog values of said differential data signal pair and having an output representative of a digital binary state of said differential data signal pair~~.

2. (Previously Presented) The comparator circuit of Claim 1, wherein said reference combiner comprises:

a first controlled current source having an input coupled to a

first signal of said differential data signal pair;

a second controlled current source having an input coupled to a second signal of said differential data signal pair; and

a current summing junction for summing an output of said first controlled current source and an output of said second controlled current source for providing said reference value.

3. (Previously Presented) The comparator circuit of Claim 2, wherein said single-ended comparator comprises a third controlled current source having an input coupled to said single-ended input and an output coupled to said current summing junction for comparing said analog value of said single-ended data signal to said reference value.

4. (Previously Presented) The comparator circuit of Claim 3, wherein said first controlled current source comprises a first transistor having a gate coupled to said first signal of said differential data signal pair, wherein said second controlled current source comprises a second transistor having a gate coupled to said second signal of said differential data signal pair, and wherein said third controlled current source comprises a third transistor having a gate coupled to said single-ended input.

5. (Previously Presented) The comparator circuit of Claim 4,

further comprising a fixed current source coupled to said current summing junction, whereby said comparator detects a difference between said analog value of said single-ended signal and an average of said analog values of said first signal and said second signal of said differential data signal pair.

6. (Previously Presented) The comparator circuit of Claim 4, further comprising a first resistance coupled to a second channel connection of said third transistor, whereby a gain of said output of said single-ended comparator is determined.

7. (Currently Amended) The comparator circuit of Claim 6, further comprising a differential comparator circuit for comparing said analog values of said differential data signal pair, wherein said differential comparator circuit comprises a fourth transistor having a gate coupled to said first signal of said differential data signal pair, a fifth transistor having a gate coupled to said second signal of said differential data signal pair and a first channel connection coupled to a second resistance for providing active mode operation, a second current source coupled to a channel connection of said fourth transistor and a second channel connection of said fifth transistor, whereby said differential comparator detects a difference between said first signal and said second signal of said differential data signal pair, and wherein

said first resistance has a resistance value twice that of said second resistance, whereby a gain of said active mode of said differential comparator is equal to a gain of said single-ended comparator.

8. (Previously Presented) The comparator circuit of Claim 2, wherein said first controlled current source comprises a first transistor having a gate coupled to said first signal of said differential data signal pair, and wherein said second controlled current source comprises a second transistor having a gate coupled to said second signal of said differential data signal pair.

9. (Previously Presented) The comparator circuit of Claim 8, further comprising a fixed current source coupled to said current summing junction, whereby said reference combiner supplies a current in conformity with an average of said analog values of said differential data signal pair to said fixed current source.

10. (Currently Amended) A method for detecting a single-ended signal, said method comprising:

receiving a single-ended data signal;

receiving a differential data signal pair;

combining both signals of said differential signal pair to provide a reference value; ~~and~~

comparing an analog value of said single-ended signal to said reference value, whereby a binary logic state of said single-ended signal is detected in conformity with analog values of both signals of said differential signal pair~~; and~~

~~second comparing said analog values of said pair of differential data signals to each other to provide a differential pair detected output indicative of a binary logic state of said differential data signal pair~~.

11. (Previously Presented) The method of Claim 10, wherein said combining comprises:

controlling a first controlled current source with an analog value of a first signal of said differential data signal pair;

controlling a second controlled current source with an analog value of a second signal of said differential data signal pair; and

summing an output of said first controlled current source and an output of said second controlled current source to provide said reference value.

12. (Previously Presented) The method of Claim 11, wherein said comparing comprises controlling a third controlled current source with said single-ended data signal, and wherein said summing further sums an output of said third controlled current source.

13. (Previously Presented) The method of Claim 12, wherein said summing further sums a current supplied by a fixed current source, whereby said comparing detects a difference between said analog value of single-ended signal and an average of said analog value of said first signal and said analog value of said second signal of said differential data signal pair.

14. (Previously Presented) The method of Claim 12, further comprising converting a current result of said summing to a voltage via a first resistance, whereby said comparing is performed in an active mode, producing a voltage substantially linearly proportional to a difference between said reference value and said analog value of said single-ended signal in a region where said reference value and said analog value of said single-ended signal are substantially equal.

15. (Currently Amended) The method of Claim 14, <u>further comprising second comparing said analog values of said pair of differential data signals to each other to provide a differential pair detected output,</u> wherein said second comparing produces a second voltage via converting a difference current to said second voltage via a second resistor, and wherein said first resistor has a resistance substantially twice that of said second resistor, whereby a gain of said first comparing and a gain of said second

comparing are substantially equal.

16. (Currently Amended) A comparator circuit, comprising:

a pair of differential inputs for receiving a differential data signal pair;

a single-ended input for receiving a single-ended data signal;

a first transistor having a gate coupled to a first signal of said differential signal pair;

a second transistor having a gate coupled to a second signal of said differential signal pair;

a third transistor having a gate coupled to said single-ended input; ~~and~~

a fixed current source coupled to a common connection of a first channel connection of each of said first transistor, said second transistor and said third transistor, whereby said single-ended data signal is compared to a common-mode value of said differential signal pair, and wherein an output provided from a second channel connection of said third transistor is representative of a binary state of said single-ended data signal~~; and~~

~~a differential comparator for comparing analog values of both signals of said differential data signal pair with each other and having an output representative of a digital binary state of said differential data signal pair~~.

17. (Previously Presented) The comparator circuit of Claim 16, further comprising a first resistance coupled to said second channel connection of said third transistor, whereby a first gain of a single-ended output of said comparator is determined in an active region of operation of said comparator.

18. (Currently Amended) The comparator circuit of Claim 17, further comprising ~~wherein said differential comparator comprises~~:

a fourth transistor having a gate coupled to said first signal of said differential data signal pair;

a fifth transistor having a gate coupled to said second signal of said differential data signal pair;

a second fixed current source coupled to a common connection of a first channel connection of each of said fourth transistor and said fifth transistor, whereby said first signal and said second signal of said differential data signal pair are compared; and

a second resistance coupled to a second channel connection of said fifth transistor, whereby a gain of a differential output of said comparator is determined, and wherein a resistance value of said first resistance is substantially twice a resistance value of said second resistance, whereby said first gain is equal to a second gain of said differential output in an active region of

operation.

RECORD OF TELEPHONIC INTERVIEW

On January 12, 2005, an interview was conducted with Primary Examiner Kenneth Wells. Both Andoh, et al. (U.S. 5.936,466) and Alexander, et al. (U.S. 5,936,469) were discussed with respect to the rejection of the Claims in the above-referenced Office Action, as well as in the Parent Application 09/870,623. As recorded in the Examiner's Interview Summary for the Parent Application mailed on January 14, 2005, it was agreed that neither Andoh nor Alexander disclose or suggest a single-ended data input signal, and therefore the invention as claimed patentably defines over the cited references.

An Amendment is entered above, and the Primary Examiner agreed that the removal of the differential comparator from Claims 1 and 16 and the removal of the second comparing the differential signals in Claim 10 would still distinguish the invention from the references, as the amendment above essentially restores the claims to the condition presented in response to the Examiner's Office Action of March 25, 2004, in which all of the claims included the above-recited limitation of a single-ended data input signal, and in particular, detecting the binary state of the single-ended data signal in conformity with a common mode voltage of a differential data signal pair.